Professor Avi (Abraham) Mendelson

CURRICULUM VITAE

Date: July-2023

1 Personal Details

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2 Higher Education

A. Undergraduate and Graduate Studies

Period of Study	Name of Institution and Department	Degree	Year of Approval of Degree
1987—1990	Electrical Engineering Department, University of Massachusetts at Amherst	Ph.D	1990
1980 -1982	Computer Science Department, Technion	.MSC	1982
1975—1979	Computer Science Department, Technion	BSC	1979

3 Academic Ranks and Tenure in Institutes of Higher Education

Dates	Name of Institution and Department	Rank/Position
2016- 2020	EE Department, NTU University (Singapore)	Visiting (Full) Professor
2011 - Current	Technion -- CS departments	Visiting (full) professor
2015 – 8.2017	Kinneret Collage	Professor (full), head of the EE department.
2004 - 2011	Technion -- EE and CS departments	Adjunct Senior Teaching Fellow
2000 - 2004	Technion -- EE and CS departments	Adjunct Senior Lecturer
1998 - 1999	Technion -- EE department	Adjunct Lecturer
1991 - 1998	Technion -- EE department	Lecturer

4 Offices in Academic Administration

2011 – 2016 Head of the Nvidia Center of Education (together with Prof Mark Silberstein), Technion

2011 – Current Member of the Parallel System Lab. In both CS and EE departments, Technion

1994 – 1998 Head of the Parallel system Lab, EE Department, Technion

5 Scholarly Positions and Activities outside the Institution

5.1 Membership:

- IEEE Fellow
- ACM, IEEE, IEEE-Computer society

5.2 Editorial:

- 2019-current Associate Editor, IEEE Transactions on Emerging Topics in Computing
- 2014 – 2019 Associate Editor, IEEE Transactions on Computers
- 2010 – 2014 Associate Editor, IEEE Computer Architecture Letters

5.3 Award committees and special committees

- 2020 – current IEEE Computer Society Chapter -- Israel
- 2017 – 2019 IEEE Computer Society Board of Governor
- 2017 – 2018 Chair of the Eckert-Mauchly awards committee
- 2015 – 2017 Member of the Eckert-Mauchly Awards Committee
- 2013 – Current Member of the Computer Science Advisory Board to Ministry of Education, Israel
- 2013 – Current Member of the CECL (manage the ACM chapter activities in Europe)
- 2013 – 2014 Head of the ACM distinguished member committee (together with Prof. Lorry Clark)
- 2010 – 2014 Member of the ACM distinguished member committee
- 2009 - 2014 Member of the ACM-Europe Council (full term)

5.4 Advisory Boards (Academic)

- 2016 – 2018 Advisory Board of the RoMoL (ERC Grant)
- 2013 – 2017 Advisory board of ISCA conference (the main conference for Computer Architecture)
- 2008 – 2013 Member of the advisory board of Microsoft Lab in BSC, Barcelona
- 2008 – 2016 Member of the industrial board of HiPEAC network of excellence

5.5 Referee:

Every year I am doing 20-30 paper reviews for leading Journals and conferences

5.6 Program Committee of major conferences

Participants in more than 30 program committees of major conferences, including

- International Conference on Computer Architecture (ISCA)
- Architecture that supports Programming languages and operating systems (ASPLOS)
- International Conference on Microarchitectures (MICRO)
- International Conference of parallel Architecture and Compilers (PACT)

- High-performance Embedded systems and architecture (HiPEAC)
- Parallel and Distributed Computing and Networks (PDCN).
- ACM international conference on Supercomputing (ICS)

5.7 Participation in Scholarly Conferences

(In this section I am providing only "samples" of the different talks, invited distinguished talk and similar activities I was part)

a. **Active Participation – Panelist, Keynote and invited talks**

International

Date	Name of Conference	Place of Conference	Subject of Lecture/Discussion	Role
2023	**AAI2023**	**Serbia**	**Opportunities and Challenges of the ChatGPT Era**	**Keynote**
2023	**HARRIS 2023**	**Germany**	**GNN based Reverse Engineering**	**Invited talk**
2022	**Mateo 2022**	**Spain**	**Computer Architecture – Past-Present-Past?**	**Invited talk**
2019	**MAST - Micro-Architectural Security**	**Madras, India**	**New concepts in micro-architecture for security design**	**Keynote**
2017	**IEEE AI/Machine Learning & Cybersecurity Confluence**	**Philadelphia, USA**	**AI/Machine Learning & Cybersecurity Confluence**	**By invite participation**

2016	**RoMoL**	**Barcelona**	Panel on the future of Runtime systems	**Panelist**
2015	**EMC²**	**Viena**	Power managements in parallel embedded systems	**Invited talk**
2015	**Conf. on Medical devoces**	**China**	Innovation – Technology for the Society	**Invited talk**
2014	**SIAT institute**	**China**	The challenge of Fault-Tolerance mechanisms for power-efficient massive parallel systems	**Invited talk**
2014	**HiPEAC**	**Barcelona**	HiPEAC's impart on the Academic and Industry in Europe"	**Invited talk**
2014	**DAC Conf.**	**Germany**	GPGPU for dependable systems – a blessing or a curse?	**Keynote speech**
2013	International symposium on Computer Architecture and High Performance Computing	**France**	The Challenge of Fault-Tolerance Mechanisms for Power-efficient Massive Parallel Systems	**Keynote speech**
2013	ISCA	**Tel-Aviv**	Opening and Closing remarks for ISCA'2013	**Duty as a general chair**
2010	Multicore workshop	**Barcelona**	Will SW cope with the developing paste of parallel HW?	**Panelist and moderator**
2009	Distinguish lecture serious	**Illinois, USA**	Industrial and Research Challenges in the Area of Multi-Core and Many Cores	**Keynote speech**

2008	Date	**Germany**	Issues and Challenges in Dependable Embedded Systems	**Invited talk**
2007	ICS	**USA**	Multi-cores, many-cores and special cores	**Keynote speech**
2006	IMSS	**USA**	Memory management challenges in the power-aware computing era	**Keynote speech**

In Israel

Date	**Name of Conference**	**Place of Conference**	**Subject of Lecture/Discussion**	**Role**
2016	**Metro**	**Haifa**	Processing Real-time Streaming Data	**Invited talk**
2006	**IBM workshop**	**Haifa**	How many cores are too many cores	**Invited talk**

b. **Organization of Conferences or Sessions**

Date	**Name of Conference**	**Place**	**Subject of Conference**	**Role**
2020	**SeHAS**	Bologna, Italy	**Secure Hardware, Architectures, and Operating Systems**	**Co-organizer and PC co-PC chair**
2019	**SPACE**	Gujarat India	**Cyber Security and Privacy**	**CO-Program chair**
2018	**ICS**	Beijin, China	**Supercomputer**	**CO-Program chair**
2013	**ISCA conference**	ISRAEL	**International symposium on computer Architecture**	**General Chair**

2010	**ICS**	Greece	**Supercomputer**	**Program committee co-chair**
2008	**ICS**	Japan	**Supercomputer**	**Program committee co-chair**
2007	**PACT**	USA	**Parallel architecture and compilers**	**Tutorial chair**

6 Awards

- 2017- IEEE Fellow
- IAA -- Inter Achievement Award (Highest award in Intel) for leading the CMP architecture for Core Due family
- "2016 Top-10 patent" for Huawei corporation

7 Invited Lectures\ Colloquium Talks

Date	Place of Lecture	Name of Forum	Presentation/Comments
2020, 2021	**Virtual workshop**	**The use of machine learning for hardware Security**	**This workshop was organized and run by Prof. Avi Mendelson and Dr. Shivam Bhasin (NTU Singapore)**
2019	**Singapore**	**MediaTek workshop**	**Secure and speculative core – how to build a secure core that perform**
2017	**Barcelona**	**Distinguish lecture**	**NVDRAM a new technological evolution or a new system revolution?**
2016	**Munich**	**Keynote in "multiprocessors for embedded systems"**	**Hardware and software mechanisms for Thermal &**

			Power/Energy management in modern multi-core systems
2015	**OSLO**	**HiPEAC Conf. keynote speach**	**Heterogeneous systems – a blessing or a curse for massive parallel dependable systems?**
2015	**China (Hangzhou)**	**West-Lake Conference**	**Keynote speech: "Sociotechnology as a drive for innovation**
2014	**UC Irvin - USA**	**Distinguished lecture series**	**The future of heterogeneous massive parallel systems**
2014	**Italy**	**ACACIS (summer school on systems)**	**Course (5 talks) on cloud computing**
2004	**Italy**	**ACACIS (summer school on systems)**	**Course (5 talks) on low power design**

8 Research Grants

a. Grants Awarded

Role in Research	Body granted	Co-Researchers	Topic	Funded by/ Amount	Year
PI	UAE	8 different universities are involved in this research avtivity	ZERO-Trust for real-time systems	850K$	2023-2026
PI	HPE (USA)		Architecture for training huge machin learning models	60K$ (this year)	2023 (may be extended)
PI	PAZI	Shahaf Vollach for Rafael	Security of real-time systems	~100K$ /year	2020-2023
PI	Cyber Security Center		4 topics	~100K$ /Yead	2020-2022
PI	Magneton with CEVA	Dr. Chaim Baskin	Quantization of mach learning algorithms	150K$	2021-2022
PI	NRF Singapore	NTU, NTS and few companies	SoCure – Building aa Secure SoC	10M $Sing	2019-2024
PI	Hundayi	Prof. Alex Bornstein	Building anti-adversa attacks on neural net	400K$	2019-2020
PI	DoD Israel		Reverse Engineering (Security)	500K Shekel for the first year	2019-2020 (hopefully will be extended)
PI	DoD Israel		Reverse Engineering (Security)	350K Shekel for the first year	2017 (hopefully will be extended)

PI	**Ministry of Science, Israel Gov.**	**From the Technion, Prof. Assaf Schuster was co-PI**	**Metro450:**	**~700K$**	**2011-2016**
Subcontractor	**European commissioner (EU)**	**100 companies. The only one from Israel**	EMC^2: support for the automotive indu	**20KE**	**2015-2017**
PI	**European commissioner (EU)**	**8 institutes around Europe. From Israel the only PI**	EuroLab-4-HPC: Foundations of a European Research Center of Excellence in High Performance Computing Systems	**Horison 2020** **100KE** **(for 2 years, but will be extended)**	**2015-2017**
PI	**European commissioner (EU)**	**EU project. From Israel the only PI**	EU FET (research project) project: Teraflex –future massive parallel systems (>1000 cores).	**EU PF7 350KE**	**2009 - 2012**
PI	**European commissioner (EU)**	**EU Project. In the Technion with Prof. Assaf Schuster**	EU IP project: Encore: Project, build a data-flow based server system	**EU PF7** **450KE**	**2009 - 2012**
PI	**European commissioner (EU)**	**EU Project. In the Technion with Prof. Israel Cidon**	EU IP project: Venus-c: Project, build a cloud infrastructure in Europe	**EU PF7** **200KE**	**2009-2011**
PI	**Intel**	**Intel Grant**	Computer architecture	**30K$**	**2002 - 2005**

$-US-Dollar. E-Euro. Shelel-Israeli local currency

9 Teaching

a. Courses Taught in Recent Years

These are some of the courses I though

Year	Name of Course	Type of Course	Degree	Number of Students
2020-current	Computer Architecture	Lecture	Undergraduate	150-200
2017-current	Architecture to support machine learning	Lecture	Graduate level, Technion	~50 -70
2019-2021	Architecture for machine learning	Lecture	Graduate level in NTU Singapore	~50 students
2016--Current	Hardware Security	Lecture	Graduate level	20-30
2018	Computer Architecture and machine learning	Lecture	Graduate level, NTU Singapore	40
2015-2017	Real-time systems	lecture	Graduate level, Technion	20-30 each time
2012 - 2017	Heterogeneous systems	Lecture	Graduate level, Technion	30-55 each time
2015	Digital Systems	Lecture	Undergraduate Technion	300
2013-1014	Operating Systems	Lecture	Undergraduate Technion	300 each time
~2010 2013	Cloud Computing	Lecture/Seminar	Graduate level, Technion	30

– 2008 2012	**Low power computers**	**Lecture**	**Graduate level, Technion**	**30**
2000 - 2008	**Computer Architecture**	**Lecture**	**Undergraduate Technion**	200-300 **each time**

10 Supervision of Graduate Students

PHD

#	Name of Student	Title of Thesis	Degree	Date of Completion / in Progress	Students' Achievements
1	Freddy Gabbay	Value prediction techniques for advanced superscalar computers	**PhD**	**1997**	**Graduated**
2	Efraim Rotem	Power management in Heterogeneous systems	**PHD**	**2015**	**Graduated**
4	Uri Verner	The use of GPGPUs for handling streaming data	**PhD**	**2015**	**Graduated**
5	Gil kedar	Schedule for power in real-time based systems	**PhD**	**2017**	**Graduated**
6	Hamad Yasin	Power and performance monitoring of large systems	**PhD**	**2019**	**Graduated**
7	Leonid Azriel	**Hardware Security**	**Ph.D**	**2020**	**Graduated**
8	Chaim Baskin	AI accelerators	**PhD**	**2021**	**Graduated**
9	Yaniv Nemcovsky	Adversarial Attacks on CNN networks	**PhD**	**In Progress**	
10	Roman Melitz	Anomaly detection in real-time systems	**PhD**	**In Progress**	

MASTER (MSC)

1	Ayelet Bak	An extension of the analytical cache model"	**MSC**	**1993**	**Graduate**
2	Avi Bitan	Asymptotic performance evaluation of computer memory models"	**MSC**	**1993**	**Graduate**
3	Zimmerman Ofer	Write cache as alternative to write back caches	**MSC**	**1994**	**Graduate**
4	Naftaly Ramaty	The use of fault tracking for debugging real-time applications	**MSC**	**1995**	**Graduate**
5	Ohad Falik	Using buffers as an alternative to caches in parallel architectures	**MSC**	**1995**	**Graduate**
6	Gabbay Freddy	TOMESI - A new cache coherency protocols for distributed multi-cache systems	**MSC**	**1995**	**Graduate**
7	Shavit Nira	New approach for load balance in Network based computer systems	**MSC**	**1996**	**Graduate**
8	Bekerman Michael	Design alternatives for	**MSC**	**1996**	**Graduate**

		multi-streams architectures			
9	Vinov Michael	The use of inter-instructions parallelism and its use for designing new architectures	**MSC**	**1996**	**Graduate**
10	Menaker Ohad	Survey on multi-threaded systems and applications	**ME**	**1997**	**Graduate**
11	Oleg Kosyakovsky	Using feedback directed optimizations to reduce power and improve performance of trace-cache systems	**MSC**	**2002**	**Graduate**
11	Assad Khamaisee	Integrating Value prediction and trace cache techniques	**MSC**	**2003**	**Graduate**
12	Shomar Bishara	Fragmented line cache – a new cache structure for saving bus bandwidth	**MSC**	**2003**	**Graduate**
13	Alexander Gendler	New hybrid based data prefetching techniques	**MSC**	**2005**	**Graduate**
14	Oren Katzengold	The use of “non executable machine instructions (Pragma) for improving the	**MSC**	**2006**	**Graduate**

		utilization of the processor resources			
15	Avi Timor	Re-execution – adding support for soft error recovery at the processor level	**MSC**	**2006**	**Graduate**
16	Behar Michael	Filter trace cache	**MSC**	**2006**	**Graduate**
17	Ishay Geler	Advance predetching techniques	**MSC**	**2007**	**Graduate**
18	Ron Gabor	Scheduling and fairness in multi core – shared memory systems	**MSC**	**2007**	**Graduate**
19	Iris Sorani	Characterization of long-traces and their applications	**MSC**	**2008**	**Graduate**
20	Shmulik Zobel	Power and performance issues in GPU architectures	**MSC**	**2010**	**Graduate**
21	Chen Damishian	New cache prefetching mechanism	**MSC**	**2010**	**Graduate**
22	Anton Lavron	Hybrid Dataflow + control flow execution model	**MSC**	**2011**	**Graduate**
23	Roman Malits	New scheduling algorithm for Graphics processors	**MSC**	**2011**	**Graduate**

24	Igor Tolchinsky	Tile Affinity	**MSC**	**2013**	**Graduate**
25	Gad Yuval	Next generation of DSP architectures	**MSC**	**2013**	**Graduate**
26	Idan Igra	User provided code for conflict resolution in transactional memory	**msc**	**2013**	**Graduate**
27	Leonid Azriel	The use of peripheral I/O processor	**MSC**	**2014**	**Graduate**
28	Ahmad Yasin	Enhanced performance and power monitoring techniques	**MSC**	**2015**	**Graduate from Haifa University**
29	Rami Jeissy	Power efficient scheduling in Heterogeneous systems	**MSC**	**2015**	**Graduate**
30	Chaim Baskin	Streaming processors	**MSC**	**2017**	**Graduate**
31	Amit Fucks	Fault tolerant OS for 1000's cores on Die system	**MSC**	**2018**	**Graduate**
32	Leor Bar-Lev	Fault tolerant mechanisms on NoC	**MSC**	**2018**	**Graduate**
33	Oren Nishri	PUF architecture	**MSC**	**2018**	**Graduate**
34	Natalie Katz	CANBUS architecture	**MSC**	**2018**	**Graduate**

35	Natan Liss	Design methodologies for FPGA	**MSC**	**2019**	**Graduate**
36	Orit Faina	Security models	**MSC**	**2019**	**Graduate**
37	Uri Shomroni	Using machine learning to manage resources of computer systems	**MSC**	**2019**	**Graduate**
38	Alex Karbachevsky	“Roofline” for machine learning	**MSC**	**2020**	**Graduated**
39	Dan Richer	New direction for implementing value prediction	**MSC**	**2020**	**Graduated**
40	Tal Rozen	Machine learning	**MSC**	**Graduated**	**2022**
41	Yehonatan Lusky	Machine learning and Hardware Securiy	**MSC**	**In Progress**	**2021**
42	OR Feldman	Improving WL in GNN	**MSC**	**Graduated**	**2021**
43	Kfir Girshtein	Simulation of security attacks on real-time systems	**MSC**	**C**	**2023**
44	Dani Kogen	GNN subgraph matching	**MSC**	**In progress**	**2021**
45	Ron Segev	Remote side channel attacks	**MSC**	**About to Graduated**	**2023**

46	Ron Alfia	Multimodal for automotive applications	**MSC**	**In progress**	**2022**
47	Liad Gerstner	Computer Architecture to support the training of huge machine learning models.	**MSC**	**In Progress**	**2022**
48	Moshe Kimchy	Quantization training	**MSC**	**Graduated**	**2023**
49	Nathaniel Rothschild	NAS	**MSC**	**In progress**	**2022**

11 Professional Experience

PROFESSIONAL EXPERIENCE

- 2015 - Current CTO Optitura LTD**.**
- 2016 –2018 Consultant to Shannon Labs, Huawei, China
- 2013 – 2015 Consultant to Shannon Labs, Huawei, China
- 2009 - 2012 Microsoft R&D Israel, manager of the Academic outreach and external research, Israel
- 1999 - 2009 Intel, Principle Engineer, architect for future micro-architecture, mobility Group, Israel

  His role included
  - Senior member of the research group
  - Architect of the CMP features in Core Due family – got the IAA (Inter Achievement Award) for this work
  - Work on accelerators and different GPGPU aspects (HW and SW)
  - Part of the small team that worked on the definition of next generation processor architecture (2015)
- 1997 – 1999 National Semiconductors, Head of the PC research Lab, senior chip architect and a senior member of the PC-on-a-chip (GEOD) team

- 1979 – 1990 Rafael- Director of a software engineering group and in charge of research in Object Oriented techniques and formal methods for developing real-time systems

SIGNIFICANT PROFESSIONAL PROJECTS (part of his industrial activities)

- Architect of the CMP feature of Intel Core-Due family of processors. These work considered to be a break-through in the design of modern processors, since was the first one to trade frequency with multiple cores on die, since we understood that power will govern the design of modern architectures**.**
- As part of my work in Intel, I was deeply involved in the process of defining the power management support for the CMP architectures such as in Core-Due family**.**
- Few of the research topics I initiated and lead while in Intel research (MRL) were implemented few years later and are part of the current products or most likely will be part of the next generation cores**.**
- Part of the architecture team of the first “System-on-Chip” National produce. This work considered to be a breakthrough in designing System-On-Chip (SoC) architecture. The design included revolutionary aspects of mixed-signal design, integration methodologies, new testing methodologies, new SW/HW interfaces and more
- Help to design of Next Generation Data-Center for Huawei Shannon Lab
- PI in the SoCure project, a 10MS$ aiming at building a secure SoC based system.

12 PUBLICATIONS

12.1 Refereed papers in professional journals

1. A. Mendelson, D.K. Pradhan and A.D. Singh: "A single cache copy data coherence (sccdc) scheme for multiprocessor systems", in Computer Architecture Notes, PP 36-49, December 1989.
2. A. Mendelson, D. Thiebaut and D.K. Pradhan : "Modeling live and dead lines in cache memory systems", in IEEE Trans. on Computers, pp. 1-16, Jan. 1993.
3. A. Mendelson and S. Pinter and R. Shtokhamer,: "Optimization techniques for cache based instruction caches", in Computer Architecture Notes, April 1994. (and in Lecture Notes in Computer Science, No. 786, Springer-Verlag, April 1994, pp. 404--418.)
4. M. Bekerman and A. Mendelson :"A performance Analysis of Pentium Processor Systems", IEEE Micro, October 1995, pp 72 -83.
5. F. Gabbay and A. Mendelson : "Using Value Prediction to increase the Power of Speculative Execution Hardware", in ACM Transactions on Computer Systems Vol. 16, No. 3 (Aug. 1998), Pages 234-270
6. F. Gabbay and A. Mendelson : "Improving Achievable ILP through Value Prediction and Program Profiling." Microprocessors and Microsystems, vol.22, no.6, November 30. 1998. Pages 315-332
7. F. Gabbay and A. Mendelson : "The "Smart" simulation Environment -- A tool-set to Develop New Cache Coherency Protocols", Journal of System Architecture 45 (1999) pp 619-632
8. A. Mendelson and M. Bekerman : "Design Alternatives of Multithreaded Architecture.", Journal of Parallel systems and programming (IJPP), 27(3) Aug. 1999. Pages 161-193.

9. N. Suri and A. Mendelson, : "Design of a Parallel Interconnect Based on Communication Pattern Considerations" Journal of Parallel Algorithms and Applications, Vol 16, Sept 2001, pp 243-271
10. Avi Mendelson and Freddy Gabbay: "The Effect of Seance Communication on Multiprocessing Systems" in ACM Transaction on Computer Systems, V-19 I-2 May 2001**,** pp 252-281.
11. Ronny Ronen, Avi Mendelson, Konrad Lai, Shih-Lien Lu, Fred Pollack, and John P. Shen: "Coming Challenges in Microarchitecture and Architecture" in Proceedings of the IEEE , Volume: 89 Issue: 3 , March 2001 Page(s): 325 -340
12. A. Roth and R. Ronen and A. Mendelson: "Dynamic techniques for load and load-use scheduling" in Proceedings of the IEEE , Volume: 89 Issue: 11 , Nov. 2001, Page(s): 1621 –1637
13. Baruch Solomon, Avi Mendelson, Ronny Ronen, Doron Orenstein, Yoav Almog: Micro-operation cache: a power aware frontend for variable instruction length ISA. IEEE Trans. VLSI Syst. 11(5): 801-811 (2003)
14. A. Cohen, L. Finkelstein, A. Mendelson, R. Ronen, D. Rudoy. "On Estimating Optimal Performance of CPU Dynamic Thermal Management." IEEE computer Architecture Letters, V2, Oct. 2003.
15. Alexander Gendler and Avi Mendelson and Yitzhak Birk, "A PAB-Based multi-prefetcher Mechanism", International Journal of Parallel Programming" 34(2): 171-188 (2006).
16. Simcha Gochman, Avi Mendelson, Alon Nave and Efraim Rotem, "Introduction to Intel® Core™ Duo Processor Architecture" in Intel Technology Journal, Volume 10, issue 02, pp 89-98 2006.
17. Avi Mendelson, Julius Mandelblat, Simcha Gochman, Anat Shemer, Rajshree Chabukswar, Erik Niemeyer, Arun Kumar "CMP Implementation in systems based on the Intel® Core™ Duo Processor Architecture", in Intel Technology Journal, Volume 10, issue 02, pp 99-108 2006.

18. Alon Naveh, Efraim Roterm, Avi Mendelson, Simcha Gochman, Rajshree Chabukswar, Karthik Krishnan, Arun Kumar , "Power and Thermal Management in the Intel® Core™ Duo Processor Architecture" in Intel Technology Journal, Volume 10, issue 02, pp 109-122, 2006.
19. Alex Gontmakher , Assaf Schuster and Avi Mendelson: Inthreads: a low granularity parallelization model, in ACM SIGARCH Computer Architecture News, v.34 n.1, p.77-80, March 2006
20. M. Behar , A. Mendelson and A. Kolodny, " Trace Cache Sampling Filter", in ACM Trans. Computer. Systems, V25, N1, PP 28-35, 2007.
21. R. Gabor , S. Weiss and A. Mendelson, " Fairness Enforcement in Switch on Event Multithreading", ACM Transactions on Architecture and Code Optimization (TACO), Volume 4 , Issue 3 (September 2007)
22. R. Gabor , S. Weiss and A. Mendelson, "Service Level Agreement for Multithreaded Processors" ACM Transactions on Architecture and Code Optimization, Volume 6, Issue 2 (June 2009)
23. Z. Guz , E. Bolotin, I. Keidar, A. Kolodny, A. Mendelson, and U. Weiser, "Many-Core vs. Many-Thread Machines: Stay Away From the Valley", in Computer Architecture Letters, January-June 2009 (vol. 8 no. 1), pp. 25-28
24. Timor , A. Mendelson, Y. Birk and N. Suri, "Using Under-Utilized CPU resources to Enhance its Reliability" IEEE Trans. Dependable Sec. Comput. 7(1): 94-109 (2010)
25. R Malits , E Bolotin, A Kolodny, A Mendelson, "Exploring the limits of GPGPU scheduling in control flow bound" applications ACM Transactions on Architecture and Code Optimization (TACO) 8 (4), 29
26. Rotem, E. ; Ginosar, R.; Weiser, U.; Mendelson, A. "Energy Aware Race to Halt: A Down to EARtH Approach for Platform Energy Management". IEEE Computer Architecture Letters – pp 1-4, Oct 2012
27. R. Giorgi et al., "TERAFLUX: Harnessing dataflow in next generation teradevices", Microprocessors and Microsystems 01/2014; http://dx.doi.org/10.1016/j.micpro.2014.04.001

28. Leonid Azriel , Avi Mendelson, Uri C Weiser, “Peripheral Memory: a Technique for Fighting Memory Bandwidth Bottleneck”, in *IEEE Computer Architecture Letters*, vol. 14, no. 1, pp. 54-57, Jan.-June 1 2015
29. Efraim Rotem, Ran Ginosar, Avi Mendelson, Uri C. Weiser “Power and thermal constraints of modern system-on-a-chip computer” Microelectronics Journal, Elsevier, December, 2015, pp 1225-1229
30. S. Weis, A. Garbade, B. Fechner, A. Mendelson, R. Giorgi and T. Ungerer: “Architectural Support for Fault Tolerance in a Teradevice Dataflow System”, International Journal of Parallel Programming (IJPP), Springer, February, V2, PP 218—232, 2016
31. Rotem Efraim, Uri C. Weiser, Avi Mendelson, Ran Ginosar, Eli Weissmann, Yoni Aizik, Intel Corporation “H-EARtH: Heterogeneous Multi-Core Platform Energy Management” special issue of IEEE Computer, on Energy-Efficient Computing, 49 (10), 47-55 , 2016
32. Uri Verner, Avi Mendelson, Assaf Schuster, "Extending Amdahl's Law for Multicores with Turbo Boost", IEEE Computer Architecture Letters, 16 (1), 30-33
33. Jawad Haj-Yihia, Ahmad Yasin, Yosi Ben Asher, and Avi Mendelson, “Fine-Grain Power Breakdown of Modern Out-of-Order Cores and Its Implications on Skylake-Based Systems.”, in *ACM Trans. Archit. Code Optim.* 13, 4, Article 56 (December 2016)
34. G. Kedar, A. Mendelson and I. Cidon, "SPACE: Semi-Partitioned CachE for Energy Efficient, Hard Real-Time Systems," in IEEE Transactions on Computers, vol. 66, no. 4, pp. 717-730, April 1 2017.
35. Leonid Azriel, Ran Ginosar and Avi Mendelson, “Using Scan Side Channel to Detect IP Theft” –IEEE Transactions on VLSI, 25(12), 3268-3280, 2017
36. Zhibin Yu, Wen Xiong, Lieven Eeckhout, Zhendong Bei, Mendelson Avi, Chengzhong Xu, “MIA: Metric Importance Analysis for Big Data Workload

Characterization", IEEE Transactions on Parallel and Distributed Systems 29 (6), 1371-1384, 2018

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